

Fig.3

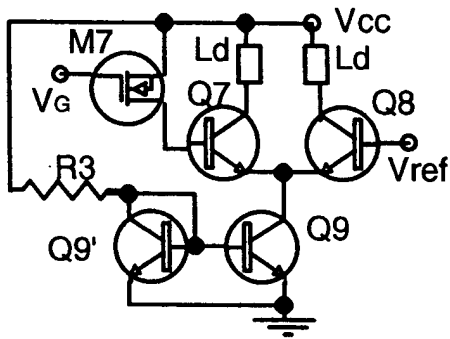


Fig.4a

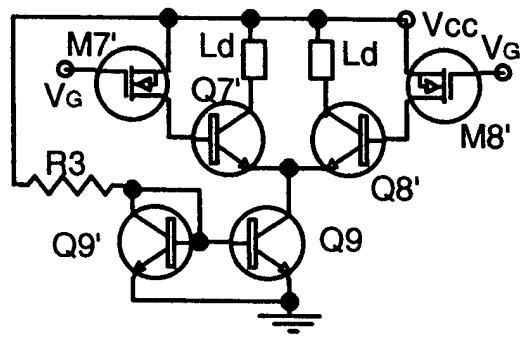


Fig.4b

Common source			
M7	M7'	M8'	Gate
D7	D7'	D8'	Substrate

Fig.5a

Common source			
M7	M7'	M8'	Gate
D7	D7'	D8'	Substrate

Fig.5b